CLAIMS

We Claim:

1 A method for reconfiguring a memory array, comprising:

(a) providing the memory array as at least one row of single-port cells up to a first metal layer;

(b) coupling a split word line having first and second word lines to the single-port cells in each row, wherein the first word line is patterned in the first metal layer, and the second word line is patterned in a second metal layer;

(c) coupling the split word line to a spacer cell in the row; and

(d) programming the base memory array into custom configurations based on whether the first and second word lines are connected over the spacer cell, or whether the first and second word lines are left unconnected.

2 The method of claim 1 wherein step (d) further includes the step of: providing a single-port configuration by connecting the first and second word lines over the spacer cell using the second metal layer or higher.

3 The method of claim 2 wherein step (d) further includes the step of: providing a dual-port configuration by,

(i) interconnecting internal nodes of respective pairs of adjacent single-port cells in the row using the second metal layer to reconfigure the single-port cells into dual-port cells, and

(ii) leaving the first and second word lines unconnected over the spacer cell.

4 The method of claim 1 wherein step (d) further includes step of: providing a single-port, no break configuration in which the first word line is coupled to the second word line using a via 1 and metal 2 connection, and wherein the second word line extends across the spacer cell.

5 The method of claim 1 wherein step (d) further includes step of: providing a configuration comprising a break with single-port on either side in which the split word line is severed over the spacer cell to form two split word lines and therefore two sub-arrays on each side of the spacer cell, and wherein the first and second word lines in the respective split word lines are connected using via 1 and metal 2, thereby creating single-port sub-arrays on both sides of the spacer cell.

6 The method of claim 1 wherein step (d) further includes step of: providing a configuration comprising a break with single port on one side and dual port on the other side in which the split word line is severed over the spacer cell to form two split word lines and therefore two sub-arrays on each side of the spacer cell, and wherein the first and second word lines of one of the split word lines are connected using via 1 and metal 2, creating single-port sub-array on a first side of the spacer cell, while the first and second word lines of

the other split word line are left unconnected, creating a dual-port sub-array a second side of the spacer cell.

7 The method of claim 1 wherein step (d) further includes step of: providing a dual-port, no break configuration in which the split word line extends across the spacer cell and the first and second word lines are coupled using separate via 1 and metal 2 connections, providing dual-port functionality.

8 The method of claim 1 further including the step of: providing a configuration in which two single-port sub-arrays are woven together coupling the first and second word lines of the split word line extending across the spacer cell between the two sub-arrays using via 1 and metal 2 connections.

9 The method of claim 1 wherein step (d) further includes step of: providing a configuration comprising a break with dual-port on either side the split word line is severed over the spacer cell to form two split word lines and therefore two sub-arrays on each side of the spacer cell, and wherein the first and second word lines in the respective split word line are left unconnected, creating dual-port sub-arrays on both sides of the spacer cell.

10 The method of claim 1 wherein step (d) further includes steps of: providing a no break supply voltage configuration in which a metal VDD line within the

spacer cell is not broken, thereby supplying power cells on both sides of the spacer cell.

11 The method of claim 10 wherein step (d) further includes steps of: providing a break supply voltage configuration in which the VDD line within the spacer cell is severed, such that the VDD connection is turned-off to an unused portion of the base memory array, thereby preventing unused portion of the array to affect the operating portions of the array.

12 A configurable memory array, comprising:

an array of single-port cells fabricated up to a first metal layer;

a split word line having first and second word lines patterned across a plurality of rows in the array and coupled to each of the single-port cells in the row, wherein the first word line is patterned in the first metal layer, and the second word line is patterned in a second metal layer; and

columns of spacer cells fabricated in the array, wherein the split word lines of each of the plurality of rows are coupled to the corresponding spacer cell in that row;

wherein the base memory array can be programmed using the second layer of metal into custom configurations based on whether the first and second word lines of the split word lines are connected over

the spacer cell, or whether the first and second word lines are left unconnected.

13 The memory array of claim 12 wherein the columns of spacer cells can be used as break points to define sub-arrays by severing the split word lines across a particular column of spacer cells.

14 The memory array of claim 12 wherein a single-port configuration can be provided by connecting the first and second word lines over the spacer cells using the second metal layer or higher

15 The memory array of claim 14 wherein a dual-port configuration can be provided by,

(i) interconnecting internal nodes of respective pairs of adjacent single-port cells in each row using the second metal layer to reconfigure the single-port cells into dual-port cells, and

(ii) leaving the first and second word lines unconnected over the spacer cells.

16 The memory array of claim 12 wherein a single-port, no break configuration is provided in which the first word line is coupled to the second word line using a via 1 and metal 2 connection, and wherein the second word line extends across the spacer cells.

17 The memory array of claim 12 wherein a configuration comprising a break with single-port on either side is provided in which the split word lines are severed over the spacer cells to form two split word lines and therefore two sub-arrays on each side of the spacer cells, and wherein the first and second word lines in the respective split word lines are connected using via 1 and metal 2, thus creating single-port sub-arrays on both sides of the spacer cells.

18 The memory array of claim 12 wherein a configuration comprising a break with single port on one side and dual port on the other side is provided in which the split word lines are severed over the spacer cells to form two split word lines and therefore two sub-arrays on each side of the spacer cells, and wherein the first and second word lines of the split word lines are connected using via 1 and metal 2, creating single-port sub-array on a first side of the spacer cells, while the first and second word lines of the other split word lines are left unconnected, creating a dual-port sub-array on a second side of the spacer cells.

19 The memory array of claim 12 wherein a dual-port, no break configuration is provided in which the split word lines extend across the spacer cells and the first and second word lines are coupled using separate via 1 and metal 2 connections, providing dual-port functionality.

20 The memory array of claim 12 wherein a configuration comprising a break with dual-port on either side is provided in which the split word lines are severed over the spacer cells to form two split word lines and therefore two sub-arrays on each side of the spacer cells, and wherein the first and second word lines in the respective split word line are left unconnected, creating dual-port sub-arrays on both sides of the spacer cells.

21 The memory array of claim 12 wherein a no break supply voltage configuration is provided in which a metal VDD line extending across each row of the array and across the spacer cells are not broken, thereby supplying power cells on both sides of the spacer cells.

22 The memory array of claim 24 wherein a break supply voltage configuration is provided in which the VDD line across the spacer cells are severed, such that the VDD connection is turned-off to an unused portion of the base memory array, thereby preventing the unused portion of the array to affect operating portions of the array.

23 A method for reconfiguring a base memory array, comprising:

(a) fabricating a base memory array up to the metal 1 layer as an array of single-port cells, wherein the base memory includes a first word line in each row coupled to the single-port cells in that row;

(b) identifying which horizontal rows of the base array and which columns of spacer cells will be used as break points for defining sub-array boundaries;

(c) patterning a second word line along each row of the base array parallel to the pre-existing metal 1 word line using metal 2 to provide each row of the base array with a split word line pair;

(d) for any areas of the array to be configured as a dual-port sub-array, reconfiguring the single-port cells as dual-port cells by interconnecting internal nodes of respective pairs of adjacent cells in each row using via 1 and metal 2 layers;

(e) programming any required horizontal break points into the base array by severing bit lines along the identified rows;

(f) providing single-port functionality for single-port sub-arrays by using via 1 and metal 2 or higher to connect the two word lines in each split word line pair of the sub-array over within the spacer cells defining the single-port sub-array break points; and

(g) providing dual-port functionality for dual-port sub-arrays by leaving the two word lines in each split word line pair unconnected within the spacer cells defining the dual-port sub-array break points.

24 A method for reconfiguring a memory array, comprising:

(a) providing the memory array as at least one row of single-port cells prior to adding a first metal layer;

(b) coupling a split word line having first and second word lines to the single-port cells in each row, wherein the first word line is patterned in the first metal layer, and the second word line is patterned in a second metal layer;

(c) coupling the split word line to a spacer cell in the row; and

(d) programming the base memory array into custom configurations based on whether the first and second word lines are connected over the spacer cell, or whether the first and second word lines are left unconnected.

25 The method of claim 24 wherein the first metal layer is configurable, such that the first metal layer can be patterned continuously across the spacer cell.

26 The method of claim 24 wherein step (d) further includes the step of: providing a single-port configuration by connecting the first and second word lines over the spacer cell using the second metal layer or higher.

27 The method of claim 26 wherein step (d) further includes the step of: providing a dual-port configuration by,

(i) interconnecting internal nodes of respective pairs of adjacent single-port cells in the row using the second metal layer to reconfigure the single-port cells into dual-port cells, and

(ii) leaving the first and second word lines unconnected over the spacer cell.